Code: CT12 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

MARCH 2011

NOTE:

- **Question 1 is compulsory and carries 28 marks. Answer any FOUR questions from the rest. Marks are indicated against each question.**
- **Parts of a question should be answered at the same place.**

Q.1 **(7×4)**

a. (i) Convert $(1110110001101 01.0011101)_2$ to decimal, octal forms and hexadecimal form.
(ii) Add $(7320)_8$ and $(326525)_8$

b. Realise the following function using PAL.
$W = \sum 0,2,4,6,8,11$
$X = \sum 1,3,5,7,9$

c. Draw the logic diagram and the truth table for a BCD to decimal decoder.

d. Explain in detail the formats for IEEE 754 floating point representation in both single precision and double precision.

e. Subtract the following numbers using 2's complement subtraction
(i) 111001_2 from 101011_2
(ii) 101011_2 from 111001_2

f. Explain push and pop instructions with respect to stack operation in a basic computer system.

g. Write a brief note on memory hierarchy.

Q.2 a. How do you explain the computer system from the following different views:-
(i) Computer architect's view
(ii) Logic designer's view
(iii) Programmer's view **(9)**

b. Write the code to implement the expression $(A)\times(B)+(C)\times(D)$ on 3, 2, 1 address machine. **(9)**

Q.3 a. Discuss the following addressing modes with functional schematics.
(i) Displacement addressing or Indexed addressing
(ii) PC Relative addressing
(iii) Register direct addressing **(9)**

b. What is Microprogramming? With a neat block diagram explain how microprogramming control is implemented? **(9)**

Q.4 a. What is cache memory? Explain direct mapping and associative mapping methods in a cache memory system. **(9)**

b. Explain the following interrupt controlled data transfer techniques:
(i) Daisy chaining (ii) use of multiple interrupt lines
(iii) Software polling. **(9)**

Q.5 a. Discuss in detail the various bench marks available for evaluating the overall performance of a computer system. **(9)**

b. Assuming 10ns clk cycles, 4 cycles for ALU operations and branches, 5 cycles for memory operations, calculate average instruction execution time for non-pipelined processor, if relative frequency of these operations are 40%, 20% and 40% respectively. Pipeline adds 1ns overload to the clock. What is the speedup gained? **(9)**

Q.6 a. Discuss the various classifications of parallel computers. **(9)**

b. Explain the delay due to data dependency in RISC computers. **(9)**

Q.7 a. Write brief note on the following architectures:
(i) superscalar
(ii) superpipelined
(iii) VLIW architectures. **(9)**

b. Compare CISC with RISC architecture. **(9)**